

WHAT IS CLAIMED IS:

1. A semiconductor device, comprising:
a semiconductor substrate with a trench;
a particulate insulating layer filling at least a
5 lower portion of the trench and comprising insulating
particles; and
a reflowable dielectric layer covering an upper
surface of the particulate insulating layer, the
insulating particles being stable at a melting point or
10 a softening point of the reflowable dielectric layer.
2. The device according to claim 1, wherein the
reflowable dielectric layer comprises silicate glass
doped with impurity.
3. The device according to claim 1, further
15 comprising a barrier insulating layer on a sidewall and
a bottom surface of the trench.
4. The device according to claim 1, further
comprising a cap insulating layer covering an upper
surface of the reflowable dielectric layer and having a
20 melting point or a softening point higher than the
melting point or the softening point of the reflowable
dielectric layer.
5. The device according to claim 1, wherein the
particulate insulating layer further comprises an
25 insulating binder.
6. The device according to claim 1, wherein an
upper surface of the particulate insulating layer is

lower than an upper surface of the semiconductor substrate.

7. The device according to claim 1, wherein an average diameter of the insulating particles falls
5 within a range of 100 nm to 500 nm or a range of 100 nm to half a width of opening of the trench.

8. A semiconductor device, comprising:
a semiconductor substrate with a trench; and
a particulate insulating layer filling at least a
10 lower portion of the trench and comprising first and second insulating particles, an average diameter of the second insulating particles being smaller than an average diameter of the first insulating particles.

9. The device according to claim 8, further
15 comprising a barrier insulating layer on a sidewall and a bottom surface of the trench.

10. The device according to claim 8, wherein the first insulating particles form a first particulate insulating layer, and the second insulating particles
20 form a second particulate insulating layer covering an upper surface of the first particulate insulating layer.

11. The device according to claim 8, wherein the first and second insulating particles are mixed.

25 12. The device according to claim 8, further comprising a reflowable dielectric layer covering an upper surface of the particulate insulating layer, the

first and second insulating particles being stable at a melting point or a softening point of the reflowable dielectric layer.

13. The device according to claim 12, further
5 comprising a cap insulating layer covering an upper surface of the reflowable dielectric layer and having a melting point or a softening point higher than the melting point or the softening point of the reflowable dielectric layer.

10 14. The device according to claim 8, wherein the particulate insulating layer further comprises an insulating binder.

15 15. The device according to claim 8, wherein the average diameter of the first insulating particles and the average diameter of the second insulating particles fall within a range of 100 nm to 500 nm or a range of 100 nm to half a width of opening of the trench.

16. A semiconductor device, comprising:
a semiconductor substrate with a trench; and
20 a particulate insulating layer filling at least a lower portion of the trench and comprising insulating particles and an insulating binder that bonds the insulating particles together, the insulating particles and the insulating binder forming a network structure.

25 17. The device according to claim 16, further comprising a barrier insulating layer on a sidewall and a bottom surface of the trench.

18. The device according to claim 16, further comprising a reflowable dielectric layer covering an upper surface of the particulate insulating layer, the insulating particles being stable at a melting point or
5 a softening point of the reflowable dielectric layer.

19. The device according to claim 18, further comprising a cap insulating layer covering an upper surface of the reflowable dielectric layer and having a melting point or a softening point higher than the
10 melting point or the softening point of the reflowable dielectric layer.

20. The device according to claim 16, wherein an average diameter of the insulating particles falls within a range of 100 nm to 500 nm or a range of 100 nm
15 to half a width of opening of the trench.

21. A semiconductor device, comprising:
a semiconductor substrate with a trench; and
a particulate insulating layer filling at least a lower portion of the trench and including first and
20 second particulate insulating layers, the first particulate insulating layer comprising first insulating particles with no binder, and the second particulate insulating layer covering an upper surface of the first particulate insulating layer and
25 comprising second insulating particles and an insulating binder.

22. The device according to claim 21, further

comprising a barrier insulating layer on a sidewall and a bottom surface of the trench.

23. The device according to claim 21, further comprising a reflowable dielectric layer covering an upper surface of the second particulate insulating layer, the first and second insulating particles being stable at a melting point or a softening point of the reflowable dielectric layer.

24. The device according to claim 23, further comprising a cap insulating layer covering an upper surface of the reflowable dielectric layer and having a melting point or a softening point higher than the melting point or the softening point of the reflowable dielectric layer.

25. The device according to claim 21, wherein an average diameter of the first and second insulating particles falls within a range of 100 nm to 500 nm or a range of 100 nm to half a width of opening of the trench.

26. The device according to claim 4, wherein an upper surface of the cap insulating layer is flush with an upper surface of the semiconductor substrate.